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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/347,690	KHAIRA ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7-23-2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-28* is/are allowed.

6)☒ Claim(s) *1,2,10,14,16-18 and 21* is/are rejected.

7)☒ Claim(s) *3-9, 11-13, 15, 19, 20, 22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-28 have been presented for reconsideration in view of Applicants arguments.

Response to Arguments

2. Applicant's arguments filed on 7-23-2004 have been fully considered. Examiners response is as follows:

2.1 Regarding Applicants response to the 35 U.S.C. 102(b) rejections of Independent Claim 18:

Applicant argued;

> The Applicants were unable to locate the activities of "expanding the repeated circuit structure" (there is no repeated structure shown) and "grafting the expanded structure" (since there is no expanded structure) as claimed by the Applicants.

The Examiner respectfully points out that in the *Beasang* reference is the following structures are disclosed, first the Examiner notes that in **Figures 10 A and 10B** the insertion of **item 713,** the Examiner asserts that this is an *"expansion of a repeated circuit structure"* as claimed by the Applicant. Second, the Examiner notes that the *Beasang* reference teaches in **Figure 2A, item 335** that in this block is recited *"Add A New Chain to The Set"* this is functionally equivalent to *"expansion of a repeated circuit structure."* The Examiner notes that **Figure 6B** a new circuit structure, *item 652* is being grafted into another circuit structure, *item 654* and therefore is now an expanded structure.

2.2 Regarding Applicants response to the 35 U.S.C. 102(b) rejections of Independent Claim 10:

Applicant argued;

As to claim 10, it appears two elements claimed by the Applicants (i.e., "merging a plurality of extended latch boundary components into a plurality of partitions" and "maintaining a load balance within the plurality of partitions") were not addressed in the Office Action, and the Applicants were unable to find an indication of their existence in Beausang-1.

Merging boundary latch components into partitions, *note in **Figure 3B** the dotted line, hence two (or a plurality) of partitions, note that there are an equal number of number of elements in each group, hence each output of group one **Items 307** have a paired input **Items 321** hence each load of the **307** items is "balanced" with an input on the **321** items.*

2.3 Regarding Applicants response to the 35 U.S.C. 102(b) rejections of Independent Claim 17:

Applicant argued;

As to claim 17, there does not appear to be either "primary inputs" (e.g., only a single primary input 307 is shown in FIG. 3A) or "primary outputs" (none are shown) as set forth in the claim (i.e., a path comprising a plurality of first nodes selected from a group consisting of latches and primary outputs and a plurality of second nodes selected from a group consisting of latches and primary inputs, where the path can include a plurality of latches between the plurality of first nodes and the plurality of second nodes").

The Examiner notes that the Applicant has failed to *distinctly* define what a *"primary input"* is as opposed to a *"primary output"* in such a manner that clearly distinguishes over the matter disclosed in the *Beausang et al.* reference in **Figures 15A and 3B.**

2.4 Regarding Applicants response to the 35 U.S.C. 103(a) rejections of Claims 1, 21 and 14:

Applicant has argued that all of the claimed limitations have not been disclosed in these references and that the motivation to combine is improper *(see pages 9-13 in the Applicant's response dated 7-23-2004.*

The Examiner notes that all of the limitations have been mapped to the references in the rejections *(see sections 5 & 6 in this office action)*. Further, the Examiner notes that all of the 35 U.S.C. 103(a) rejections have been provided with motivations as to why these different references were combined. It is further noted by the Examiner that the *same* inventor *James Beausang* was an inventor on all three references cited.

The Examiner has found Applicant's arguments to be unpersuasive and upholds the earlier 35 U.S.C. 102(b) rejections of Claims 18, 10, 16 & 17 and the 35 U.S.C. 103(a) rejections of Claims 1, 21, 2 & 14 are upheld.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Independent **Claim 18** is rejected under 35 U.S.C. 102(b) as being anticipated by **Beausang U.S. Patent 5,828,579.**

3.1 As regards independent **Claim 18** the *Beausang* reference teaches, a method of sharing a repeated circuit structure in a circuit model **(Figure 6A, Col. 6 Lines 43-67, Col. 7 Lines 1-34),** expanding the repeated circuit structure **(Figure 6B, Col. 6 Lines 43-67, Col. 7 Lines 1-34)**; and grafting the expanded circuit structure to the circuit model **(Figure 7B, Col. 6 Lines 43-67, Col. 7 Lines 1-34).** The Examiner directs the Applicant to the term *"scan chain design database"*, as disclosed in the *Beausang* reference.

4. Independent **Claims 10, 16 and 17** is rejected under 35 U.S.C. 102(b) as being anticipated by **Beausang et al. U.S. Patent 5,903,466.**

4.1 As regards independent **Claims 10, 16 and 17** the *Beausang et al.* reference teaches, a latch boundary component **(Figure 13B Items 1050 and 1057)**, a plurality of first nodes **(Figure 15A, *note the plurality of input nodes on 1050 and 1051*)**, with a plurality of output latches, going to a plurality of input latches **(Figures 3B).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Independent **Claims 1 and 21** and dependent **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Beausang et al. U.S. Patent 5,903,466** *(hereafter referred to as*

Beausang-1) in view of **Beausang et al. U.S. Patent 5,949,692** *(hereafter referred to as Beausang-2).*

5.1 As regards independent **Claims 1 and 21** the *Beausang-1* reference discloses preparing a circuit model for simulation **(Figures 3A, 12, Col. 8 Lines 47-67, Col. 9 Lines 1-22),** decomposing the circuit model having a number of latches into a plurality **(Figures 15A and 15B),** of extended latch boundary components **(Figure 13B,** *note, Applicant's specification defines, page 3, an Extended Latch Boundary Component as being a latch with an inverter output, note items 1050 and 1057 in Figure 13B* **and Figures 16A, 16B, 17A, 17B and 18A).**

However, the *Beausang-1* reference does not expressly disclose, partitioning the plurality of extended latch boundary components, *however, it is noted by the Examiner that the Beausang-1 reference does disclose the need for linking groups of scan cells into a design to be tested (**Col. 3 Lines 10-16**).*

The *Beausang-1* reference does disclose that: *it is unclear under the prior art system when a designer can "sign off" on his or her work in the design process **(Col. 4 Lines 13-17).*** The Examiner notes, that even though there is a solution to the problem of long compile times for IC designs presented in the *Beausang-1* reference, an artisan of ordinary skill would have been motivated to find a better solution to decrease the amount of time required to compile a design and to address the express deficiencies of the *Beausang-1* reference. In the Hierarchical scan architecture art the *Beausang-2* reference discloses partitioning the plurality of extended latch boundary components **(Figure 2A Item 310, Figures 6A-14B, Col. 26 Lines 50-67, Col. 27 Lines 1-17).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the extended latch boundary components teachings of the *Beausang-1* reference with the partitioning methods of the *Beausang-2* reference because, the IC designer can now *"sign off"* his or her work at the completion of the module design and their completed and optimized modules do not need to be later disrupted ***(Beausang-2 Col. 3 Lines 3-11)***, thus reducing the amount of time required to qualify the design and increase productivity.

5.2 As regards dependent **Claim 2** the *Beausang-1* reference does not expressly disclose decomposing hierarchical cells into a plurality of extended latch boundary components.

The *Beausang-2* reference discloses decomposing hierarchical cells into a plurality of extended latch boundary components **(Figures 6A-14B).**

For the motivation to combine the Beausang-1 reference with the Beausang-2 reference please see paragraph 3.1 above.

6. Independent **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Beausang et al. U.S. Patent 5,903,466** *(hereafter referred to as Beausang-1)* in view of **Beausang et al. U.S. Patent 5,828,579** *(hereafter referred to as Beausang-3).*

6.1 As regards Independent **Claim 14** the *Beausang-1* reference discloses preparing a circuit model for simulation **(Figures 3A, 12, Col. 8 Lines 47-67, Col. 9 Lines 1-22),** having a total simulation time **(Col. 4 Lines 6-9).**

However, the *Beausang-1* reference does not expressly disclose grouping the plurality of extended latch boundary components into a plurality of partitions, *although the Beausang-1 reference does disclose extended latch boundary components,* **(Figure 13B,** *note, Applicant's specification defines, page 3, an Extended Latch Boundary Component as being a*

latch with an inverter output, note items 1050 and 1057 in Figure 13B **and Figures 16A, 16B, 17A, 17B and 18A),** and reducing the communication time within the plurality of partitions by adjusting the grouping.

The *Beausang-1* reference does disclose that: *it is unclear under the prior art system when a designer can "sign off" on his or her work in the design process* ***(Col. 4 Lines 13-17).***

The Examiner notes, that even though there is a solution to the problem of long compile times for IC designs presented in the *Beausang-1* reference, an artisan of ordinary skill would have been motivated to find a better solution to decrease the amount of time required to compile a design and to address the express deficiencies of the *Beausang-1* reference. In the Hierarchical scan architecture art the *Beausang-3* reference discloses partitioning the plurality of extended latch boundary components **(Col. 12 Lines 51-55)** as well as grouping a plurality of partitions **(Col. 12 Lines 45-48),** as well as methods of adjusting the grouping **(Col. 13 Lines 9-15, Col. 37 Lines 20-67, Col. 38, Col. 39 Lines 1-36, Figures 12A-14B).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the boundary scan teachings of the *Beausang-1* reference with the scan resource grouping teachings of the *Beausang-3* reference because, *the module designer will no be able to "sign off" his or her work at the completion of the module design (Beausang-3 Col. 3 Lines 7-12),* which will decrease the amount of communication **time** required for the modules in each of the groupings ***(Beasang-3 Col. 3 Lines 51-57).***

Allowable Subject Matter

5. The following is an Examiner's reasons for allowance: Independent **Claim 24** is allowable over the prior art of record. The combination of a *dicing unit* in combination with the partitioning of a plurality of *extended boundary latch boundary components*, including a *simulation unit coupled* to the *dicing unit*, is a non-obvious modification over the prior art of record.

5.1 Independent **Claim 28** is allowable over the prior art of record. The limitation, in combination with other limitations of, *finding each cell in the plurality of cells that is highest in the hierarchy such that a single extended latch boundary component satisfying a given size constraint can be mapped into a cell,* is not disclosed nor made obvious by the prior art of record.

5.2 Dependent **Claims 25-27** are allowed as they depend upon an allowed base claim.

5.3 Dependent **Claims 3-9, 11-13, 15, 19, 20, 22 and 23** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Applicant's arguments have been unpersuasive. Art rejections have been applied to independent **Claims 1, 10, 14, 16-18 and 21** and dependent **Claim 2.** Dependent **Claims 3-9, 11-13, 15, 19, 20, 22 and 23** have been objected to, **Claims 24-28** have been allowed over the prior art of record. This action is made **FINAL.**

6.1 THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC